AN10944

1930 MHz to 1990 MHz Doherty amplifier using the BLF7G20LS-200

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Document information

Info	Content
Keywords	RF power transistors, Doherty architecture, LDMOS, power amplifier, RF performance, Digital PreDistortion (DPD), W-CDMA, BLF7G20LS-200
Abstract	This application note describes the design and performance of a Doherty power amplifier for base stations in the 1930 MHz to 1990 MHz band using the BLF7G20LS-200 LDMOS transistor

Revision history

Rev	Date	Description
v.1	20110104	initial version

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1. Introduction

This application note describes the design characteristics and RF performance of a state-of-the-art Doherty power amplifier for base stations in the 1930 MHz to 1990 MHz band using the BLF7G20LS-200 LDMOS transistor.

The amplifier uses two BLF7G20LS-200 devices in a Doherty architecture on a Rogers 3006 PCB having a thickness of 0.64 mm (0.025”). The design ensures high-efficiency while maintaining a very similar peak power capability of two transistors combined. The input and output sections are internally matched, benefiting the amplifier design with high gain and good gain flatness and phase linearity over the frequency band of 1930 MHz to 1990 MHz.

The BLF7G20LS-200 is a seventh generation LDMOS device using NXP Semiconductor’s advanced LDMOS process.

2. Test summary

The amplifier was characterized under the following conditions:

- Network analyzer measurements for power gain (G_p), delay time (t_d) and Input Return Loss (IRL):
  - output power (P_L) = 46 dBm
  - drain-source voltage (V_{DS}) = 30 V
  - main power amplifier quiescent drain current (I_{Dq}) (main amplifier) = 1600 mA
  - gate-source voltage of peak amplifier (V_{GS}) (peak amplifier) = 0.296 V
- Standard IS-95 ACPR, gain and efficiency measurements:
  - P_L = 49 dBm
  - I_{Dq} (main amplifier) = 1600 mA
  - V_{GS} (peak amplifier) = 0.296 V
  - V_{DS} = 30 V
  - IS-95 signal (pilot, paging, sync, 6 traffic channels with Walsh codes 8 to 13, PAR = 9.7 dB at 0.01 % probability)
- Power and efficiency measurements (peak output power):
  - using a pulsed signal and measuring the 3 dB compression points with a pulse width of 12 μs, duty cycle of 10 % at V_{DS} = 30 V, I_{Dq} (main amplifier) = 1600 mA and V_{GS} (peak amplifier) = 0.296 V
- 2-carrier W-CDMA measurements demonstrating Digital PreDistortion (DPD) correction:
  - P_L = 49 dBm
  - 15 MHz spacing
  - V_{DS} = 30 V
  - I_{Dq} (main amplifier) = 1600 mA
  - V_{GS} (peak amplifier) = 0.3 V

Table 1. Performance summary

Frequency (GHz)	G_p at 49 dBm (dB)	IRL at 49 dBm (dB)	Peak output power ($P_{L(M)}$) (dBm)	Drain efficiency (η_D) at 49 dBm (%)	ACPR (IS-95) at 49 dBm (dBc)
1.93	17.11	−11.8	57.03	40.34	−39.6
1.96	17.38	−11.6	57.04	40.96	−40.6
1.99	17.32	−12.74	57.04	41.73	−41.2

3. Test circuit

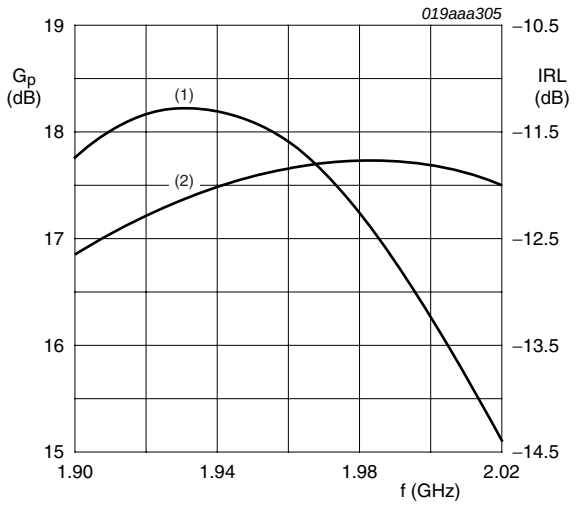
The test circuit is designed on a Rogers 3006 PCB having a thickness of 0.64 mm (0.025”), shown in Section 5 “BLF7G20LS-200 Doherty test circuit” on page 12. V_{DS} = 30 V. The gate biasing circuits are connected to the 30 V power supplies. There are 8 V regulators on the board. I_{Dq} (main amplifier) and V_{GS} (peak amplifier) can be adjusted using potentiometers.

4. RF performance

4.1 Network analyzer measurements

Network analyzer measurements were performed under the following conditions:

- P_L = 46 dBm
- V_{DS} = 30 V
- I_{Dq} (main amplifier) = 1600 mA
- V_{GS} (peak amplifier) = 0.296 V



(1) IRL.

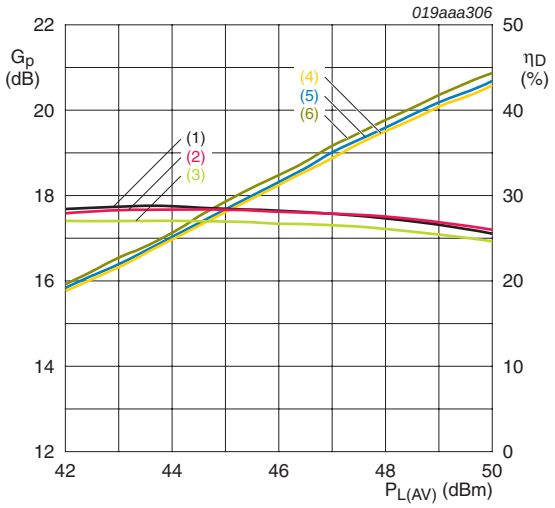
(2) G_p.

Fig 1. Power gain and input return loss as a function of frequency

4.2 IS-95 measurements

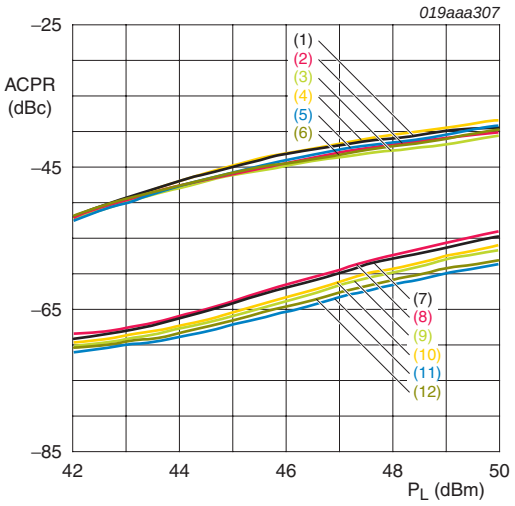
The IS-95 measurements were performed under the following conditions:

- Signal: IS-95 (pilot, paging, sync, 6 traffic channels with Walsh codes 8 to13, PAR = 9.7 dB at 0.01% probability)
- Bias: V_{DS} = 30 V
- I_{Dq} (main amplifier) = 1600 mA
- V_{GS} (peak amplifier) = 0.296 V



(1) G_p = 1930 MHz.
(2) G_p = 1960 MHz.
(3) G_p = 1900 MHz.
(4) η_D = 1930 MHz.
(5) η_D = 1960 MHz.
(6) η_D = 1990 MHz.

Fig 2. Power gain and drain efficiency as a function of average output power, IS-95



(1) 1930 MHz – 885 kHz.
(2) 1960 MHz – 885 kHz.
(3) 1990 MHz – 885 kHz.
(4) 1930 MHz + 885 kHz.
(5) 1960 MHz + 885 kHz.
(6) 1990 MHz + 885 kHz.
(7) 1930 MHz – 1.98 MHz.
(8) 1930 MHz + 1.98 MHz.
(9) 1960 MHz – 1.98 MHz.
(10) 1960 MHz + 1.98 MHz.
(11) 1990 MHz – 1.98 MHz.
(12) 1990 MHz + 1.98 MHz.

Fig 3. Adjacent Channel Power Ratio (ACPR) as a function of output power

4.3 Peak output power measurements

Peak output power was measured using a pulsed signal with a pulse width of 12 μs and duty cycle of 10 %, and measuring the 1 dB and 3 dB compression points.

The peak power measurements were performed under the following conditions:

- Bias: V_{DS} = 30 V
- I_{Dq} (main amplifier) = 1600 mA
- V_{GS} (peak amplifier) = 0.296 V

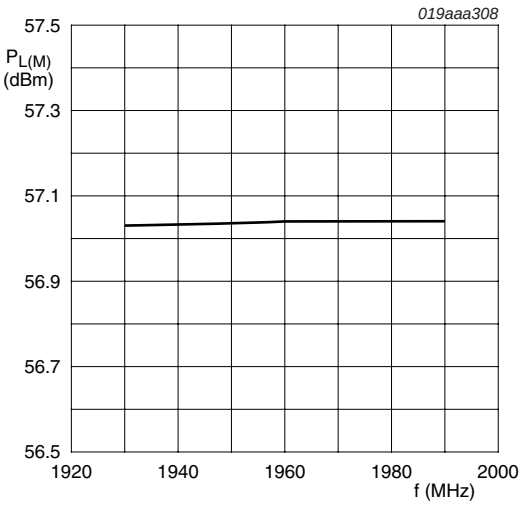
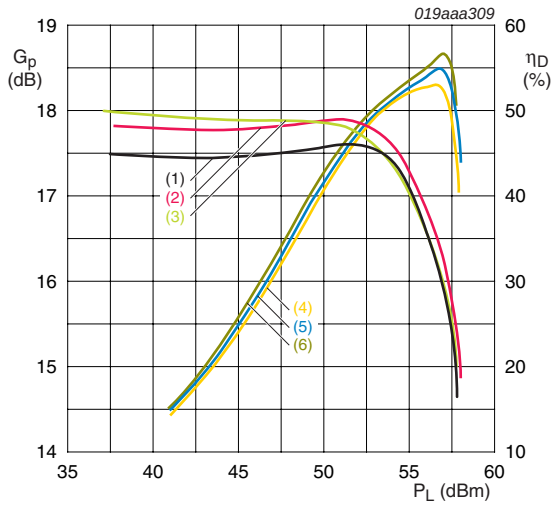


Fig 4. Peak output power as a function of frequency



(1) f = 1930 MHz.
(2) f = 1960 MHz.
(3) f = 1990 MHz.
(4) f = 1930 MHz.
(5) f = 1960 MHz.
(6) f = 1990 MHz.

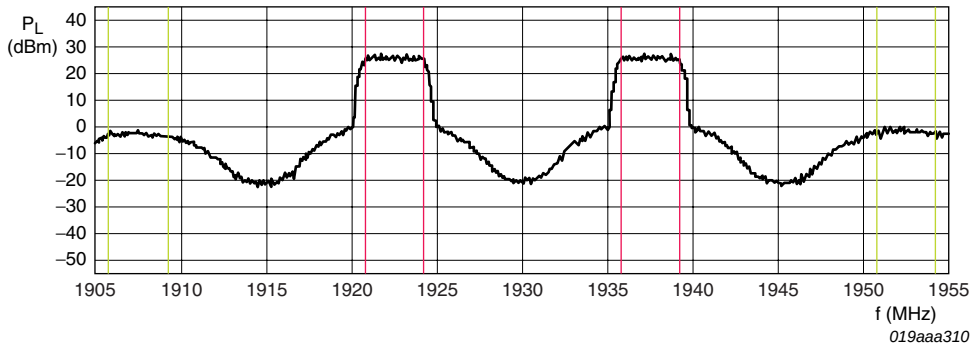
Fig 5. Power gain and efficiency as a function of output power

4.4 DPD measurements

The DPD measurements were performed using an in-house designed DPD system under the following conditions:

- f_c = 1930 MHz
- DPD system: 2-carrier W-CDMA signal, spacing: 15 MHz
- V_{DS} = 30 V, I_{Dq} (main amplifier) = 1600 mA, V_{GS} (peak amplifier) = 0.3 V

In Figure 6 to Figure 11, adjacent lower channel values are the difference in power between the channel within the LH pair of green vertical lines and the channel within the LH pair of red vertical lines. Adjacent upper channel values are the difference in power between the channel within the RH pair of green vertical lines and the channel within the RH pair of red vertical lines.



Channel 1 (reference): 46.19 dBm.

Channel 2: 46.22 dBm.

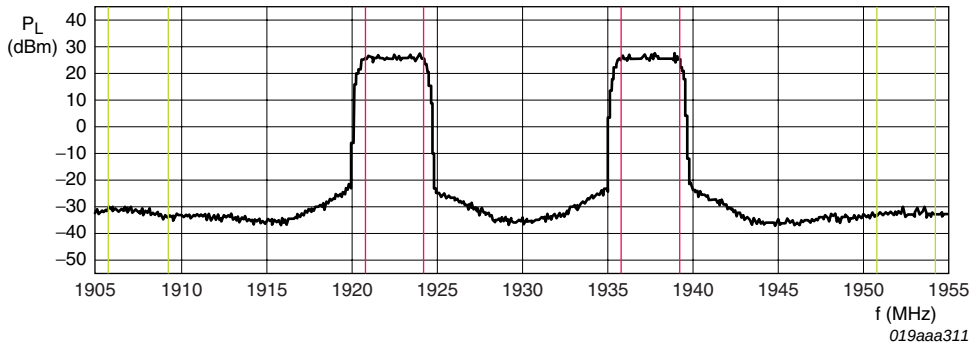
Adjacent lower channel: −28.42 dB.

Adjacent upper channel: −27.30 dB.

Total power: 49.21 dBm.

RBW: 30 kHz, VBW: 30 kHz, SWT: 2 s.

Fig 6. DPD uncorrected, f_c = 1930 MHz



Channel 1 (reference): 45.93 dBm.

Channel 2: 46.17 dBm.

Adjacent lower channel: −57.16 dB.

Adjacent upper channel: −58.08 dB.

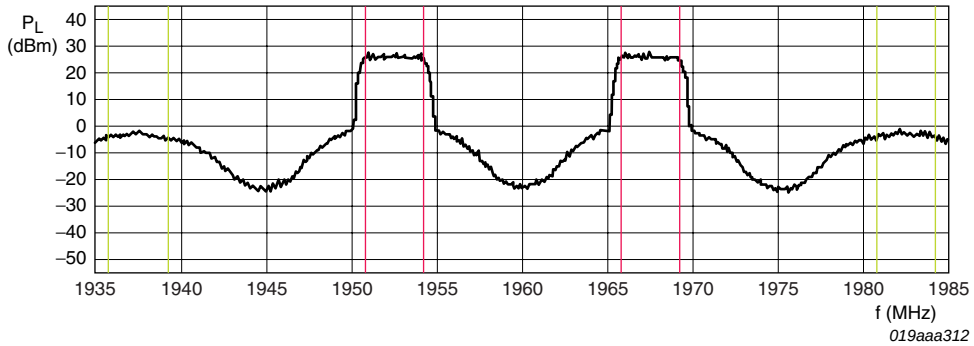
Total power: 49.06 dBm.

RBW: 30 kHz, VBW: 30 kHz, SWT: 2 s.

Fig 7. DPD corrected, f_c = 1930 MHz

The following DPD measurements were performed under the following conditions:

- f_c = 1960 MHz
- DPD system: 2-carrier W-CDMA signal, spacing: 15 MHz
- V_{DS} = 30 V, I_{Dq} (main amplifier) = 1600 mA, V_{GS} (peak amplifier) = 0.3 V



Channel 1 (reference): 45.92 dBm.

Channel 2: 45.94 dBm.

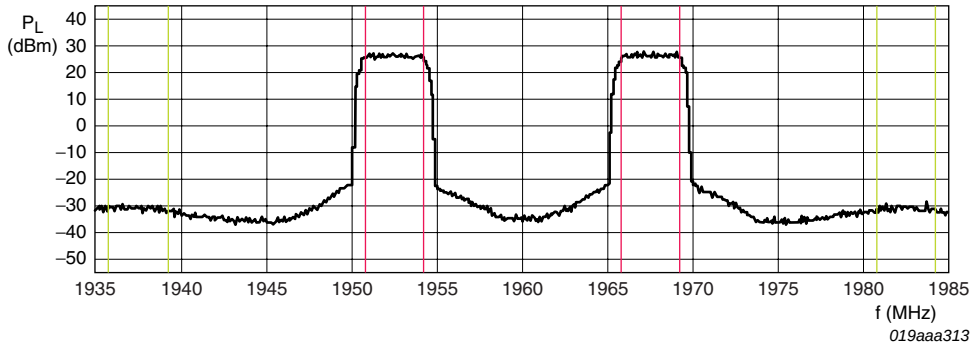
Adjacent lower channel: −29.39 dB.

Adjacent upper channel: −29.10 dB.

Total power: 48.94 dBm.

RBW: 30 kHz, VBW: 30 kHz, SWT: 2 s.

Fig 8. DPD uncorrected, f_c = 1960 MHz



Channel 1 (reference): 46.00 dBm.

Channel 2: 46.38 dBm.

Adjacent lower channel: −57.08 dB.

Adjacent upper channel: −57.11 dB.

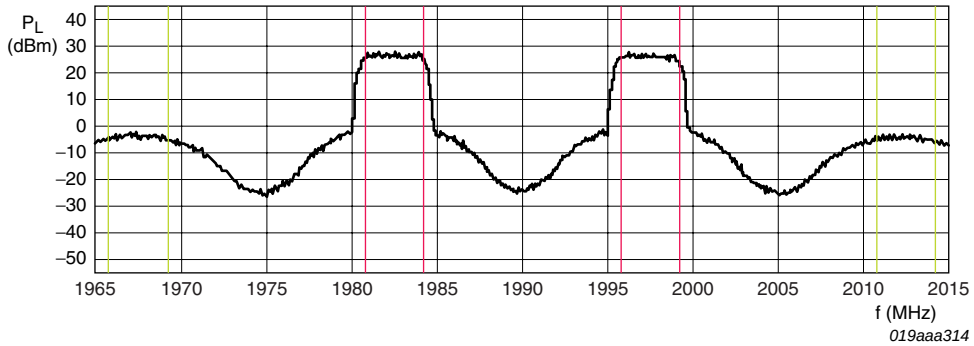
Total power: 49.20 dBm.

RBW: 30 kHz, VBW: 30 kHz, SWT: 2 s.

Fig 9. DPD corrected, f_c = 1960 MHz

The following DPD measurements were performed under the following conditions:

- f_c = 1990 MHz
- DPD system: 2-carrier W-CDMA signal, spacing:15 MHz
- V_{DS} = 30 V, I_{Dq} (main amplifier) = 1600 mA, V_{GS} (peak amplifier) = 0.3 V



Channel 1 (reference): 46.23 dBm.

Channel 2: 45.98 dBm.

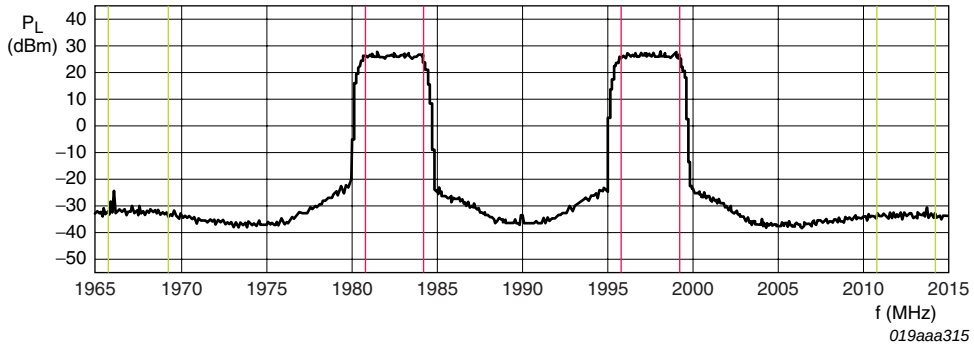
Adjacent lower channel: −30.00 dB.

Adjacent upper channel: −30.71 dB.

Total power: 49.11 dBm.

RBW: 30 kHz, VBW: 30 kHz, SWT: 2 s.

Fig 10. DPD uncorrected, f_c = 1990 MHz



Channel 1 (reference): 45.97 dBm.

Channel 2: 46.11 dBm.

Adjacent lower channel: −57.61 dB.

Adjacent upper channel: −59.37 dB.

Total power: 49.05 dBm.

RBW: 30 kHz, VBW: 30 kHz, SWT: 2 s.

Fig 11. DPD corrected, f_c = 1990 MHz

5. BLF7G20LS-200 Doherty test circuit

The test circuit is designed on a Rogers 3006 PCB having a thickness of 0.64 mm (0.025”).

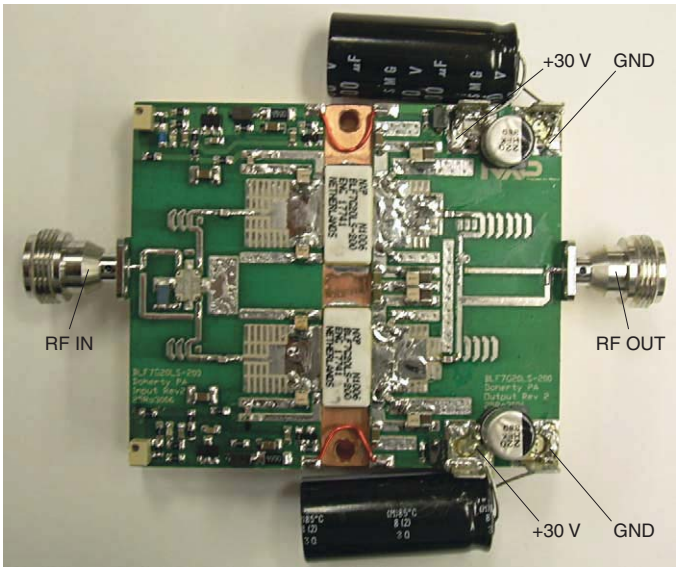


Fig 12. BLF7G20LS-200 Doherty test circuit

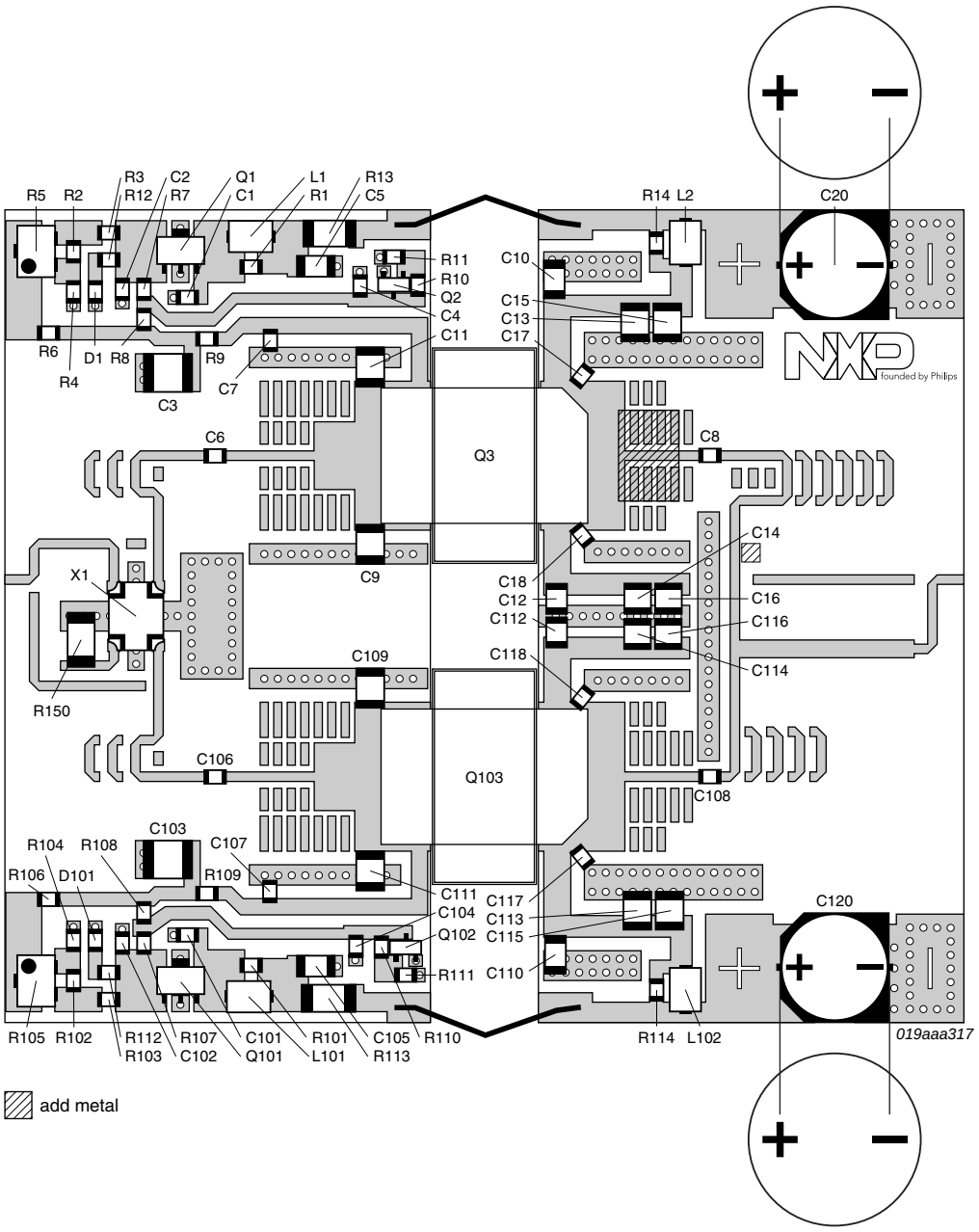


Fig 13. BLF7G20LS-200 Doherty test circuit PCB layout

5.1 BLF7G20LS-200 Doherty test circuit components

Table 2. BLF7G20LS-200 Doherty test circuit components

Designator	Description	Part identifier	Manufacturer
Input PCB	BLF7G20LS-200 Doherty PA Input-Rev2[1]	BLF7G20LS-200 Doherty PA Input 25Ro3006	Metro circuits
Output PCB	BLF7G20LS-200 Doherty PA Output-Rev2[1]	BLF7G20LS-200 Doherty PA Output 25Ro3006	Metro circuits
Q1, Q101	78L08 voltage regulator	NJM#78L08UA-ND	NJR
Q2, Q102	2N2222 NPN transistor	MMBT2222	Fairchild
Q3, Q103	BLF7G20LS-200	BLF7G20LS-200	NXP Semiconductors
R1, R14, R101, R114	9.1 Ω	CRCW08059R09FKEA	Vishay Dale
R2, R3, R102, R103	430 Ω	CRCW0805432RFKEA	Vishay Dale
R4, R104	75 Ω	CRCW080575R0FKTA	Vishay Dale
R5, R105	200 Ω, potentiometer	3214-1-201E	Bourns
R6, R106	2 kΩ	CRCW08052K00FKTA	Vishay Dale
R7, R107	1.1 kΩ	CRCW08051K10FKEA	Vishay Dale
R8, R108	11 kΩ	CRCW080511K0FKEA	Vishay Dale
R9, R109	5.1 Ω	CRCW08055R11FKEA	Vishay Dale
R10, R110	5.1 kΩ	CRCW08055K10FKTA	Vishay Dale
R11, R111	910 Ω	CRCW0805909RFKTA	Vishay Dale
R12, R112	1.1 kΩ	CRCW08051K10FKEA	Vishay Dale
R13, R113	499 Ω, 0.5 W	CRCW2010499RFKEF	Vishay Dale
X1	3 dB, hybrid coupler, 30 W	1J503S	Anaren
L1, L2, L101, L102	ferroxcube bead	2743019447	Fair Rite
C1, C2, C4, C101, C102, C104	100 nF ceramic 0805	S0805W104K1HRN-P4	MultiComp
C3, C103	4.7 μF	C4532X7R1H475M	TDK
C5, C105	1 μF	C3216X7R1H105K	TDK
C6, C7, C8, C106, C107, C108	15 pF	600F	American Technical Ceramics
C9, C11, C109, C111	0.9 pF	100B	American Technical Ceramics
C13, C14, C113, C114	15 pF	ATC100B150JT500X	American Technical Ceramics
C15, C16, C115, C116	10 μF	GRM32DF51H106ZA01L	MuRata
C10, C110	1 μF	GRM31CR72A105KA01L	MuRata
C20, C120	220 μF, 50 V electrolytic SMT	PCE3474CT-ND	Panasonic
C17, C117	2.0 pF	600F	American Technical Ceramics
C18, C118	2.4 pF	600F	American Technical Ceramics

[1] Rogers 3006; ε_r = 6.15 ± 0.15; thickness 0.64 mm (0.025”); 35 μm (1 oz.) copper on each side.

6. Abbreviations

Table 3. Abbreviations

Acronym	Description
ACPR	Adjacent Channel Power Ratio
CCDF	Complementary Cumulative Distribution Function
DPD	Digital PreDistortion
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
PCB	Printed-Circuit Board
RBW	Resolution BandWidth
SMT	Surface-Mount Technology
SWT	SWeep Time
UMTS	Universal Mobile Telecommunications System
VBW	Video BandWidth
W-CDMA	Wideband Code Division Multiple Access

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